Claims

1. Multiplier device comprising first to n^{th} multipliers M_1 to M_n for multiplying a carrier modulated information signal with first to n^{th} mutually phase shifted and identical, substantially square wave mixing signals MS_1 to MS_n with 50% duty cycle, characterized by n being greater than 2, outputs of said multipliers M_1 to M_n being respectively coupled through weighting circuits W_1 to W_n with respective fixed weighting factors WF_1 to WF_n to an adder circuit, said mixing signals MS_1 to MS_n having respective phase angles φ_i corresponding to $\varphi_i = i * \Delta\varphi$, said weighting factors WF_i corresponding to the sine value of said respective phase angles $\varphi_i = i * \Delta\varphi$ with $\Delta\varphi$ being the mutual phase difference between each two phase consecutive mixing signals corresponding to $\pi/(n + 1)$ and i varying from 1 to n.

2. Multiplier device according to claim 1, characterized by n corresponding to (N+1)/2 for an elimination of all harmonics up to the N^{th} order from the output of said adder circuit.

3. Multiplier device according to claim 1 or 2, characterized by said mixing signals MS_1 to MS_n being derived from a local oscillator signal with frequency fo through an arrangement of fixed phase shift means and/or frequency divider means.

4. Multiplier device according to claim 3, characterized by a local oscillator circuit supplying an oscillator signal with frequency fo to a serial arrangement of first to n^{th} phase shifting means, each providing a fixed phase shift of $\Delta\varphi$ and supplying respectively mixing signals MS_1 to MS_n to said first to n^{th} multipliers M_1 to M_n.

5. Multiplier device according to claim 4, characterized by said local oscillator circuit generating a clock control signal with clock frequency n *

fo being supplied through a frequency divider with dividing factor n to said serial arrangement of first to n^{th} phase shifting means, each of said first to n^{th} phase shifting means comprising a D-flip-flop being clock controlled by said clock control signal and providing said fixed phase shift of $\Delta\varphi$.